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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,337	08/06/2001	Shunpei Yamazaki	07977-211003	3550

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EXAMINER	
NELSON, ALECIA DIANE	

ART UNIT	PAPER NUMBER
2675	

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11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,337	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. The statement referencing the priority of the instant application is incorrect. The patent no of U.S. Application No. 08/997, 919 is U.S. Patent No. 6,147,667, opposed to U.S. Patent No. 6,147,919. The error appears to be a typographical error, and the examiner does acknowledge the claim for priority, however it is requested that a corrected statement be submitted in response to the office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each

claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

3. ***Claims 1-14 and 22*** are rejected under 35 U.S. C. 103(a) as being unpatentable over Sasaki et al (U.S. Patent No. 5,818,068) in view of Funai et al. (U.S. Patent No. 5,550,070).

With reference to **claim 1,** Sasaki et al. plurality of pixels (82) arranged in a matrix including source lines and gate lines, driver circuitry (84, 85) for driving the source lines and the gate lines (66, 67), and a logic circuit for processing a signal required for driving the driver circuits, buffer circuit connected to a clock signal line (64) and a start signal line (65), and the sample/hold circuit connected to the output of each buffer circuit and to the image signal line (66) (see column 12, lines 27-50), which are formed on the same insulating substrate (see column 5 lines 44-56), wherein the pixel matrix circuit, the driver circuit, and the logic circuit are constituted by a plurality of TFTs, each having an active layer comprising crystalline silicon (see column 6, lines 7-38). Further Sasaki et al. teaches that the TFT composed of the polycrystalline silicon film is formed in a manner that the directions in which the crystal grows are substantially parallel to a direction in which carriers in the film move (see column 11, line 66-column 12, line 10).

While Sasaki et al. teaches the crystals grow in a substantially parallel direction, there is no disclosure that the crystals are rod-shaped, however such shape of liquid crystal are known to those skilled in the art.

Funai et al. teaches that the crystalline silicon region (108) is made of a plurality of needle-shaped or column-shaped silicon crystals having a growth direction in parallel with the surface of the substrate (101) (see column 8, lines 55-58).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the crystal to be of rod, needle, or column-shape, as taught by Funai et al., and extending in one direction, as taught by Sasaki et al. and Funai et al. to be used in a system similar to that which is taught by Misawa and Sasaki et al. so that a leak current flowing between the shaped crystals becomes less and thereby further increasing the display characteristics and performance of the display device.

With reference to **claims 2-4,** Funai et al. further teaches that in the crystalline silicon film (110), the needle-shaped or column-shaped silicon crystals grow in a direction represented by an arrow (125), and in each needle-shaped or column-shaped silicon crystal, no grain boundaries are present in the direction (125) (see column 10, lines 11-15).

With reference to **claims 5 and 6,** it is an obvious function of liquid crystal devices for there to be an anisotropic property between the channel length direction and a channel width direction of the active layer, as well as there is and intrinsic or substantially intrinsic channel form region of the active layer.

With respects to **claims 7 and 8,** Sasaki et al. teaches that the metal element for enhancing crystallization includes at least one selected from the group consisting of nickel, iron, cobalt, palladium, and platinum. Sasaki et al. fails to teach the specific amount in usage, however the amount of metal element used is designers choice.

With reference to **claim 9,** Funai et al. teaches a gate insulating film (113) is formed on the crystalline silicon film (112), and a gate electrode (114) is formed on the gate insulating film (113). Further it is taught that in the case where the amorphous silicon film (103), the high-concentration nickel region (109), and the region (107) containing nickel in large concentrations are included in the crystalline silicon film (112) (see column 9, lines 45-62).

With respects to **claims 10 and 14,** the usage of plural TFT connecting to each picture element, and the usage of a phase compararator, low pass filter, ect, in a logic circuit, is well known in the art.

With respects to **claims 11-13,** Sasaki et al. teaches that the TFT circuit includes a mask layer (33) (see column 10, lines 50-65) and that the pixels include a pixel capacitance (111) and a hold capacitance (110) (see column 15, lines 9-33).

With reference to **claim 22,** Sasaki et al. teaches that the device could be an electroluminescence display device (see column 14, lines 41-54).

4. ***Claims 16-19, 21, 23, 24, and 26-34*** are rejected under 35 U.S. C. 103(a) as being unpatentable over Sasaki et al. in view of Zhang et al. (U.S. Patent No. 5,888,857).

Sasaki et al. plurality of pixels (82) arranged in a matrix including source lines and gate lines, driver circuitry (84, 85) for driving the source lines and the gate lines (66, 67), and a logic circuit for processing a signal required for driving the driver circuits, buffer circuit connected to a clock signal line (64) and a start signal line (65), and the sample/hold circuit connected to the output of each buffer circuit and to the image signal line (66) (see column 12, lines 27-50), which are formed on the same insulating substrate (see column 5 lines 44-56), wherein the pixel matrix circuit, the driver circuit, and the logic circuit are constituted by a plurality of TFTs, each having an active layer comprising crystalline silicon (see column 6, lines 7-38). Further Sasaki teaches that the TFT composed of the polycrystalline silicon film is formed in a manner that the directions in which the crystal grows are substantially parallel to a direction in which carriers in the film move (see column 11, line 66-column 12, line

10). With further reference to **claims 16 and 27**, the pixel circuit, driver circuit, and logic circuit are constituted with a plurality of N-channel type TFT and a plurality of P-channel type TFTs (see column 11, lines 23-36).

Sasaki et al. fails to teach the sub-threshold coefficients of the transistors, however does teach the usage of the N- and P-type transistors.

Zhang et al. teaches that the field effect mobility of the TFT obtained was 40 to 60 cm^2/Vs in the N channel type and 30 to 500 cm^2/Vs in the P channel type.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to include the field effect mobility of the TFT's as taught by Zhang et al. to the system as taught by Sasaki et al. to provide and improved semiconductor device with better reliability and performance.

With reference to **claims 23, 24, 29, 32, and 34,** Sasaki et al. teaches that the device could be an electroluminescence display device (see column 14, lines 41-54).

5. ***Claims 20 and 25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. in view of Hirakata (U.S. Patent No. 5,959,599).

Sasaki et al. plurality of pixels (82) arranged in a matrix including source lines and gate lines, driver circuitry (84, 85) for driving the source lines and the gate lines (66, 67), and a logic circuit for processing a signal required for driving the driver circuits, buffer circuit connected to a clock signal line (64) and a start signal line (65), and the sample/hold circuit connected to the output of each buffer circuit and to the

image signal line (66) (see column 12, lines 27-50), which are formed on the same insulating substrate (see column 5 lines 44-56), wherein the pixel matrix circuit, the driver circuit, and the logic circuit are constituted by a plurality of TFTs, each having an active layer comprising crystalline silicon (see column 6, lines 7-38). Further Sasaki teaches that the TFT composed of the polycrystalline silicon film is formed in a manner that the directions in which the crystal grows are substantially parallel to a direction in which carriers in the film move (see column 11, line 66-column 12, line 10).

Sasaki et al. fails to teach the amount of voltage needed to drive the gate insulating film of the TFT when it is at a certain thickness.

Hirakata teaches an active matrix type liquid-crystal display unit which in the case of using silicon oxide 1200 angstrom in thickness as a gate insulation film, there are very little elements which are destroyed in a stage where a voltage between the gate and the source is up to 10 V (see column 10, lines 29-33). Further it would be obvious to one having ordinary skill in the art to apply a higher operating voltage to the gate insulating film when the film is thicker as opposed to the amount applied when the film is thinner.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to add the applied voltage levels as taught by Hirakata, to the system as taught by Sasaki et al. to thereby provide an active matrix type liquid crystal display unit in which power consumption is reduced and very little elements are destroyed by applying a higher voltage to the thinner film.

With reference to **claim 25,** Sasaki et al. teaches that the device could be an electroluminescence display device (see column 14, lines 41-54).

Response to Arguments

6. Applicant's arguments with respect to claim1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/AND
June 1, 2004

DENNIS-DOON CHOW
PRIMARY EXAMINER